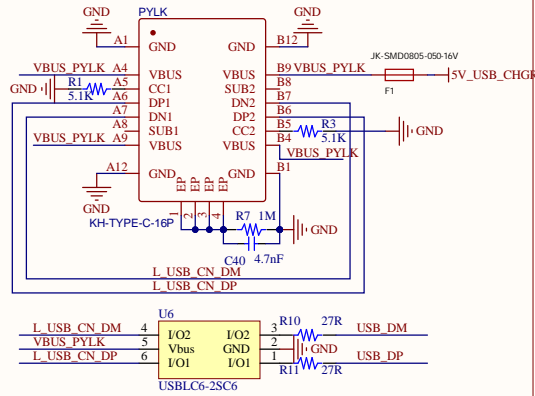
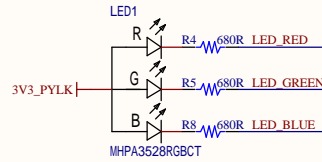


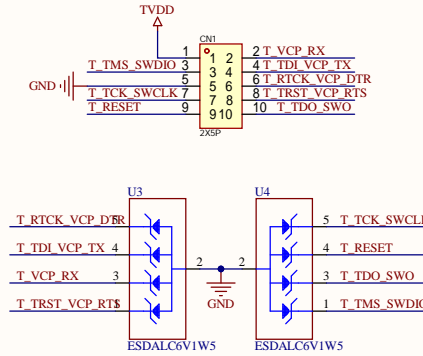
USB



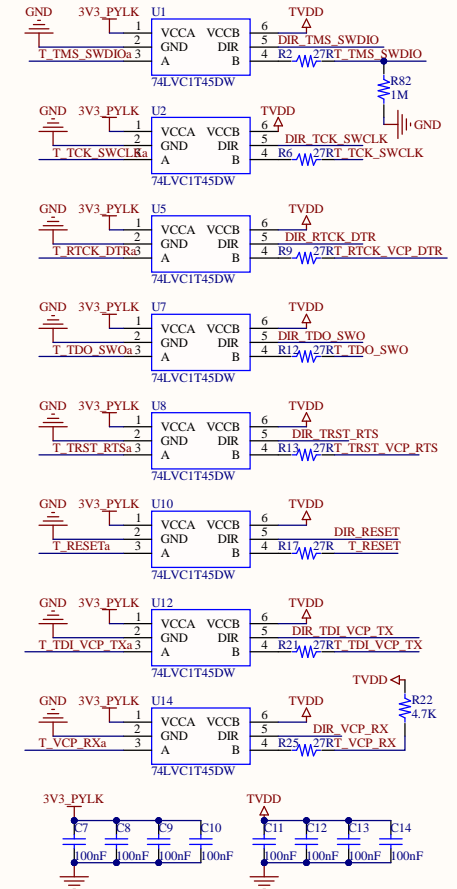
LED



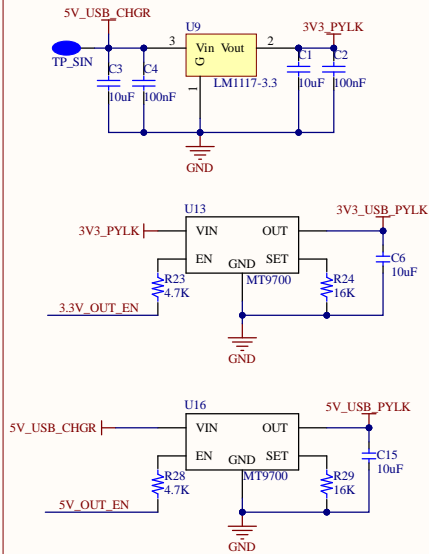
Debug Connector



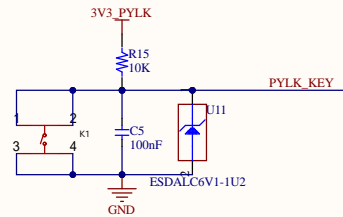
Level Shift



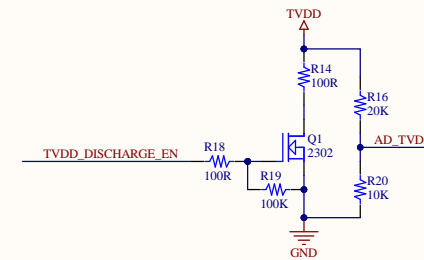
Power



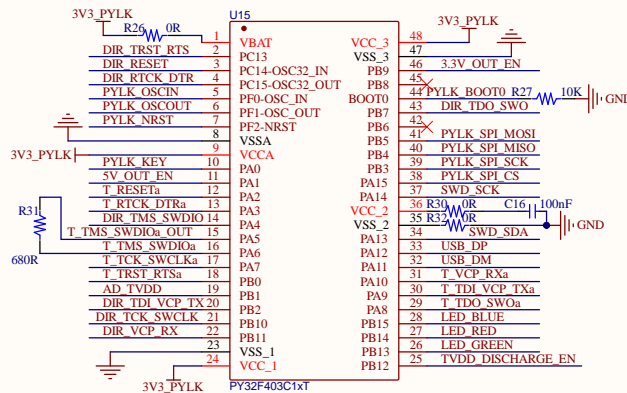
Key



ADC&Electric discharge



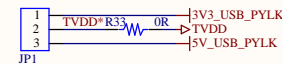
MCU



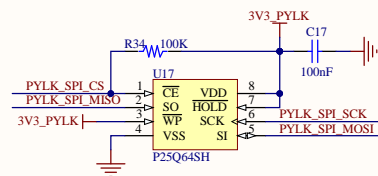
SWD



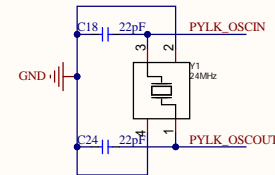
TVDD_Selection



Flash



OSC



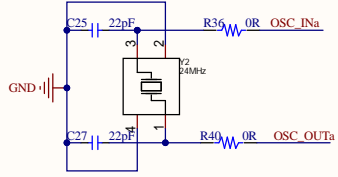
When the DIR pin is set to logic high (1), the data direction is from VCCA to VCCB.
When the DIR pin is set to logic low(0), the data direction is from VCCB to VCCA

T_TMS_SWDIO	T_TMS_SWDIO
T_TCK_SWCLK	T_TCK_SWCLK
T_RESET	T_RESET
T_TDO_SWO	T_TDO_SWO
T_VCP_RX	T_VCP_RX
T_TDI_VCP_TX	T_TDI_VCP_TX
T_RTCK_VCP_DTR	T_RTCK_VCP_DTR
T_TRST_VCP_RTS	T_TRST_VCP_RTS

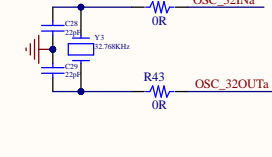


OSC

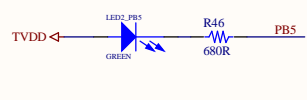
HSE



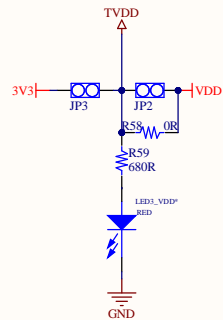
LSE



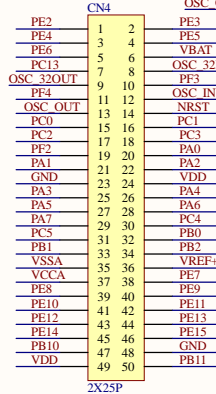
LED



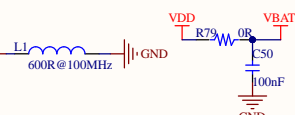
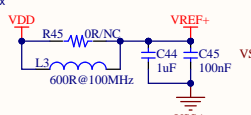
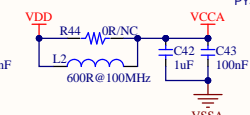
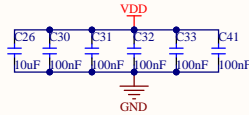
VDD_Selection



MCU



EXPENSION PIN

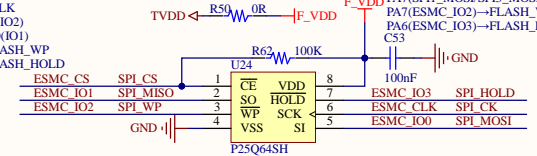


ESMC

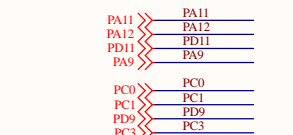
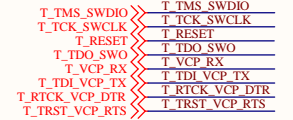


FLASH

ESMC Communication
R67, R69, R71, R73, R75, R77 weld,
R68, R70, R72, R74, R76, R78 weld,
PD2(ESMC_SS1)→CS
PA3(ESMC_CLK)→CLK
PA7(ESMC_IO0)→SL(IO2)
PB0(ESMC_IO1)→SO(IO1)
PA7(ESMC_IO2)→FLASH_WP
PA6(ESMC_IO3)→FLASH_HOLD



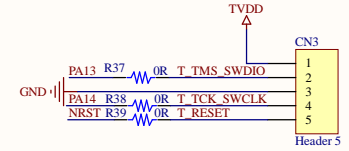
SPI



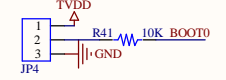
Title: PY32E407V1xT_START.SchDoc
Project: PY32E407V1xT_START.PrjPcb
Size: A3
Date: 2025/6/19
Sheet: 2 of 3
Revision: V2.1



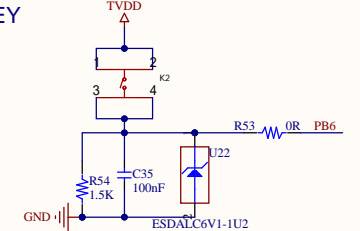
Debug Connector



BOOT_OPTION



USER_KEY



NRST

